REMARKS

Claims 1-13 are pending in this application after this Amendment. Claims 1 and 10 are independent. In light of the amendments and remarks made herein, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

In the outstanding Official Action, the Examiner rejected claim 1 under 35 U.S.C. § 112, second paragraph. The Examiner further rejected claim 1 under 35 U.S.C. § 102(b) as being anticipated by *Muramatsu et al.* (JP 06-083731); and rejected claims 1-3 and 7 under 35 U.S.C. § 102(e) as being anticipated by *Szczebak, Jr. et al.* (USP 5,640,433). Applicants respectfully traverse these rejections.

Applicants wish to thank the Examiner for indicating that claims 4, 5, 6, 8, and 9 contain allowable subject matter.

Examiner Interview

Applicants wish to thank the Examiner for the interview conducted on May 13, 2004. During the interview, Applicants indicated to the Examiner and his supervisor that it appears from some of the comments in the outstanding Official Action that the Examiner did not fully consider the Reply filed on November 17, 2003. Additionally, Applicants presented arguments that the references as cited by the Examiner fail to teach or suggest the present invention. The Examiner and his supervisor indicated that upon the filing of Applicants' response, the Examiner will formally

consider the Applicants' arguments and respond accordingly, if necessary, in a new, non-final Official Action.

Claim Rejections - 35 U.S.C. § 112

With regard to the Examiner's rejection of claim 1 under 35 U.S.C. § 112, second paragraph, by this Amendment, Applicants have amended the claim as suggested by the Examiner. Based upon the discussions had with the Examiner, it is anticipated that the Examiner will withdraw the rejection under 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 U.S.C. § 102 - *Muramatsu et al.*

In support of the Examiner's rejection of claim 1, the Examiner asserts that *Muramatsu et al.* teaches the adjustment unit as recited in claim 1. Applicants respectfully disagree with the Examiner's characterization of this reference.

It is respectfully submitted that the disclosure of *Muramatsu et al.* is directed to a self-timed clocking transfer control circuit. *Muramatsu et al.* identifies a problem with conventional transfer control circuits as conventional transfer control circuits cannot provide the necessary control processing so as to gradually precede data on a stage by stage basis for each data transmission circuit or logic circuit when transfer timing of each data transmission circuit is to be verified or the content of processing by a logic circuit disposed between data transfer circuits is to be debugged.

Muramatsu et al. seeks to solve this problem by providing for a self-timed clocking transfer control circuit capable of switching operational modes between a mode for prohibiting or acknowledging transfer operation in a desired timing and a mode for performing usual self-synchronous type of transfer control operation.

In contrast, the present invention as set forth in claim 1, as amended, recites, *inter alia*, a data transmission line, used continuously, connected in a plurality of stages in an asynchronous system, comprising a data holding unit receiving and holding data transmitted from a preceding stage or data output from an external synchronous system and an adjustment unit for adjusting timing of input of one of the data output from the synchronous system or the data transmitted in the asynchronous system from the preceding stage to the data holding unit, by the transfer control unit, when a mode in which data output from the synchronous system is taken and transmitted to the data transmission line. There is no discussion in *Muramatsu et al.* that is directed to receiving and holding data output from an external synchronous system. Further, there is no teaching or suggestion in *Muramatsu et al.* that is directed to an adjustment unit for adjusting timing of input of the data output from the synchronous system when a mode in which data output from the synchronous system is taken and transmitted to the data transmission line. As *Muramatsu et al.* fails to teach or suggest all of the claimed elements, it is respectfully submitted

that *Muramatsu et al.* fails to anticipate the present invention of claim 1. As such, it is respectfully requested that the outstanding rejection be withdrawn.

Claim Rejections - 35 U.S.C. § 102 - *Szczebak, Jr. et al.*

With regard to the Examiner's rejection of claim 1 as being anticipated by *Szczebak, Jr. et al.*, the Examiner asserts that *Szczebak, Jr. et al.* teaches the adjustment unit of the present invention as recited in claim 1, citing to Figs. 14 and 15c. Applicants respectfully disagree with the Examiner's characterization of this reference.

It is respectfully submitted that the disclosure of *Szczebak, Jr. et al.* is directed to a method and apparatus for testing telephone lines and telephone equipment such as analog private lines for voice and data communication. The system includes a circuit for converting DDS synchronous data transmissions into asynchronous transmissions, and vice versa, using a digital processor and associated circuits. A transceiver is coupled to the digital processor to receive and transmit on respective synchronous buses. The processor is connected to an asynchronous bus for receiving and transmitting asynchronous data. The positive and negative polarity pulses of synchronous transmissions received by the receiver are converted to separate pulses and coupled to the digital processor, as well as clock signals recovered from the synchronous transmission. The clock signals provide an interrupt to

the digital processor to process the synchronous pulses and convert the same to an asynchronous format.

In contrast, the present invention as set forth in claim 1 recites, *inter alia*, a data transmission line, used continuously, connected in a plurality of stages in an asynchronous system, comprising an adjustment unit for adjusting timing of input of one of the data output from the synchronous system or the data transmitted in the asynchronous system when a mode in which data output from the synchronous system is taken and transmitted to the data transmission line. It is respectfully submitted that there is no teaching or suggestion in the reference that teaches or suggests adjusting timing of input when a mode signal in which data output from the synchronous system is taken and transmitted to the data transmission line. As *Szczebak, Jr. et al.* fails to teach or suggest all of the elements of the claimed invention, it is respectfully submitted that claim 1 is not anticipated by *Szczebak, Jr. et al.* As such, it is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claims 2-9 are allowable for the reasons set forth above with regard to claim 1 at least based upon their dependency on claim 1.

By this Amendment, Applicants have added new claims 10-13. It is respectfully submitted that claim 10 contains elements similar to those discussed above with regard to claim 1, namely, claim 10

recites a mode signal to identify whether the data input to the data holding unit is synchronous data or asynchronous data, wherein the adjustment unit may adjust the timing of input of the data to the data holding unit based upon the mode signal. As set forth above, neither of the references provided by the Examiner teach or suggest this claim element. As such, it is respectfully submitted that claim 10, together with claims dependent thereon, are allowable for the reasons set forth above.

Conclusion

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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